Claims:

1. An integrated circuit comprising:

a memory array;

a test generator coupled to the memory array to generate a physical address in the memory array and to generate a test vector for the physical address wherein said test vector allows detection of a non-complaint memory cell of said memory array; and

a conversion circuit to convert the physical address in the memory array to a logical address in the memory array to allow said test vector to be written to said logical address of the memory array.

2. The integrated circuit of claim 1, wherein the conversion circuit comprises a Read Only Memory (ROM).

3. The integrated circuit of claim 1, wherein the conversion circuit comprises a Random Access Memory (RAM).

4. The integrated circuit of claim 1, wherein the conversion circuit comprises an Electrically Erasable Programmable Read Only Memory (EEPROM).

5. The integrated circuit of claim 1, wherein the test vector is capable of detecting spacial locality faults within the memory array.

6. The integrated circuit of claim 1, wherein the test vector is capable of detecting coupling transitional faults between physically adjacent memory cells.

7. A method for testing an embedded memory having memory cells, the method, comprising the steps of:

providing a test vector for a first address in the embedded memory;

determining a second address in the embedded memory based on the first address; and

writing the test vector to the second address to detect non-functional memory cells represented by the second address.

8. The method of claim 7, further comprising the step of reading the second memory address written to detect non-functioned memory cells.

9. The method of claim 7, wherein the first address is a physical memory address of the embedded memory.

10. The method of claim 9, wherein the second address is a logical memory address of the embedded memory.

11. The method of claim 7, wherein a Read Only Memory (ROM) device holds the second address of the embedded memory based on the first address generated for the embedded memory.

12. The method of claim 7, wherein a Random Access Memory (RAM) device holds the second address of the embedded memory based on the first address generated for the embedded memory.

13. The method of claim 7, wherein said testing of the embedded memory comprises neighborhood pattern sensitive testing.

14. The method of claim 7, wherein said testing of the embedded memory comprises march pattern testing.

15. In a memory array having a physical mapping scheme distinct by at least one bit from its logical mapping scheme, a method for performing built-in self-test on the memory array, the method comprising the steps of:

generating a physical row address for the memory array;

generating a logical row address for the memory array based on the physical row address; and

performing the built-in self-test on the memory array based on the generated logical row address.

16. The method of claim 15 further comprising the step of, performing the built-in self-test on a selected cell of the memory array based on the generated logical row address.

17. The method of claim 15 further comprising the step of, performing the built-in self-test on a selected memory block of the memory array based on the generated logical row address.

18. The method of claim 15, wherein an integrated circuit generates the logical row address for the memory array based on the physical row address for the array.

19. The method of claim 18, wherein the integrated circuit is a Read Only Memory (ROM) device.

20. The method of claim 18, wherein the integrated circuit is a Random Access Memory (RAM) device.

21. The method of claim 18, wherein the integrated circuit is an Electrically Erasable Programmable Read Only Memory (EEPROM).

22. The method of claim 15, wherein the built-in self-test comprises Neighborhood Pattern Sensitive Tests.

23. The method of claim 15, wherein the built-in self-test comprises March Tests.

24. A semiconductor device comprising:

a test circuit; and

a conversion circuit, coupled to said test circuit wherein the test vector circuit provides a physical memory row address for a selected group of memory cells under test to the conversion circuit for conversion of the provided physical memory address to a logical memory address for the selected group of memory cells under test.

25. The semiconductor device of claim 24, wherein the conversion circuit comprises a Read Only Memory (ROM).

26. The semiconductor device of claim 24, wherein the conversion circuit comprises a Random Access Memory (RAM).

27. The semiconductor device of claim 24, wherein the conversion circuit comprises an Electrically Erasable Programmable Read Only Memory (EEPROM).

28. The semiconductor device of claim 24, wherein the test circuit provides a test vector capable of detecting spacial locality faults within the selected group of memory cells under test,

29. The semiconductor device of claim 24, wherein the test circuit provides a test vector capable of detecting coupling transitional faults between physically adjacent memory cells within the selected group of memory cells under test.